Intelligent Bandwidth Allocation Technology Key to Efficient Operation of DAQ Systems

All-in-One DAQ Solutions at Doewe Technologies

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With the continuous growth in demand for high-bandwidth, high-precision, multi-channel synchronous testing in smart manufacturing, automotive electronics, aerospace, and new energy equipment, PXIe data acquisition systems have rapidly expanded from R&D laboratories to production lines and field debugging scenarios. The parallel quantity of acquisition boards and dedicated processing modules continues to increase, and single-channel sampling rates have surged from the megahertz level to the gigabit level, leading to exponential growth in data traffic per second. Against this backdrop, the backplane PCI Express bus has evolved from a traditional "sequential channel" into a "core hub" handling massive parallel throughput. Located at the topological center, the PXIe controller must not only handle CPU computation, I/O management, and clock synchronization but also dynamically schedule bus link resources to avoid bottlenecks and latency. Its bandwidth allocation strategy, link adaptation capability, and switching architecture design critically impact the real-time performance, throughput, and system reliability of the entire machine.

Figure 1 Side View of Doewe PXIe Controller

When evaluating the comprehensive performance of a PXIe controller, factors such as processor architecture (core count, frequency, cache hierarchy), memory capacity and bandwidth, and sustained read/write capabilities of the local storage subsystem should be comprehensively considered. These hardware parameters determine instruction execution efficiency, data buffering depth, and task scheduling margin. However, from a system-level perspective, the true constraints on overall throughput are the link width, effective transmission rate, and dynamic bandwidth allocation mechanism of the backplane PCI Express bus. The backplane bandwidth acts as the artery of the DAQ system, responsible for transferring parallel data streams between acquisition boards, processing boards, and storage media. If the link topology is fixed and cannot adapt to service loads on demand, local links may easily become congested during peak periods, leading to increased DMA transaction delays, forced reductions in sampling rates, or even buffer overflows. Meanwhile, other links may be underutilized, leaving overall bandwidth idle, thereby degrading system throughput and affecting real-time performance and data integrity. Thus, beyond providing sufficient raw bandwidth, the PXIe controller must also possess link adaptation and fine-grained bandwidth scheduling capabilities to maintain efficient and stable operation in multi-board parallel, high-data-flow application scenarios.

To overcome the bandwidth bottleneck of fixed link topologies, the ASMC-PXIe-1216 implements intelligent bandwidth allocation on its built-in PCIe switch chip: After power-on, the firmware first reads the LINK training results of the chassis backplane to dynamically grasp the negotiated width and rate of each root link. It then automatically configures the switch chip into dual-path mode (1 × 16 + 1 × 8) or quad-path mode (4 × 4) based on the detected topology and service load. During operation, if link utilization becomes unbalanced or acquisition boards are hot-swapped, the firmware dynamically rebalances forwarding paths, ensuring high-speed links always serve the boards with the highest bandwidth demands, while low-speed links handle auxiliary data streams. Through this adaptive scheduling mechanism, the controller optimizes backplane bandwidth utilization without altering physical connections, significantly reducing DMA transaction latency and CPU interrupt load, thereby fully unleashing system performance for multi-board parallel acquisition and storage.

To meet the demands of multi-board parallel, high-bandwidth data acquisition for dynamic bus management, Doewe Technologies pioneered intelligent bandwidth allocation technology in its PXIe controller series: After power-on, the controller automatically detects the chassis LINK status and adaptively switches between two link modes—(1 × 16 + 1 × 8) and (4 × 4)—based on topology and load. It continuously rebalances bandwidth during operation to avoid bottlenecks and idle resources. As the flagship model of this series, the ASMC-PXIe-1216 fully integrates this technology and features multiple high-speed transmission and reliability designs, making it an ideal control core for high-channel-count synchronous acquisition scenarios.

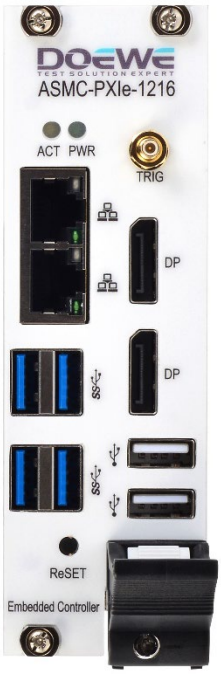

Figure 2 Front View of Doewe PXIe Controller

The ASMC-PXIe-1216 integrates a PCIe Gen3 x16 Root-Complex-based switch chip and adaptive link management firmware within a 3U dual-slot chassis: After power-on, the firmware automatically reads the chassis backplane's LINK training results and switches in real time between (1 × 16 + 1 × 8) and (4 × 4) link modes. During operation, it continuously monitors link utilization and dynamically rebalances forwarding paths, ensuring high-speed channels always serve peak-bandwidth-demand boards, thereby maintaining low DMA latency and high effective throughput. Internal P2P direct paths allow acquisition boards and high-speed storage boards to transfer large data blocks directly via the switch chip, further reducing end-to-end transmission latency in multi-board parallel operation. To support this high-speed switching architecture, the controller features an industrial COM-E processing platform, standard 16 GB DDR4 (expandable to 32 GB), a 512 GB SSD system disk, and an efficient thermal dissipation channel ensuring continuous operation at 0°C–50°C. Real-time power consumption and temperature monitoring circuits track hotspots and energy fluctuations at millisecond resolution, providing dynamic protection strategies for extreme load scenarios. External I/O includes 2 × Gigabit Ethernet, 4 × USB 3.0, 2 ×

USB 2.0, and 1 × DisplayPort (3840 × 2160 @ 60 Hz), meeting high-speed data backhaul and local HMI needs. Internally, the controller provides 16 GB/s backplane bandwidth, expanded externally to 24 GB/s via the switch chip. In multi-board parallel acquisition and high-speed storage tests, intelligent bandwidth allocation increases backplane utilization by over 40%, ensuring robust support for large-scale synchronous acquisition and long-duration high-speed recording.

Figure 3 Doewe Technologies PXIe Acquisition Card Combination

In summary, as DAQ systems enter a performance bottleneck phase dominated by bus bandwidth, dynamic link reconfiguration and inter-board P2P direct connections have become critical technologies for enhancing throughput and real-time performance. Doewe Technologies' intelligent bandwidth allocation method automatically adjusts the PCIe topology based on instantaneous loads without adding chassis slots or replacing boards. It significantly reduces transmission latency through internal switch chip passthrough mechanisms, providing stable bandwidth assurance for high-channel-count synchronous acquisition and long-duration high-speed recording. The ASMC-PXIe-1216 controller, implemented with this solution, demonstrates significant improvements in backplane utilization while maintaining low DMA latency, high link saturation, and excellent thermal stability, fully validating the effectiveness of

intelligent bandwidth scheduling in complex acquisition scenarios. For users seeking to further harness bandwidth potential and enhance sustainable operation in existing PXIe platforms, this controller offers a plug-and-play technical option and establishes a scalable hardware foundation for future large-scale data acquisition and edge real-time processing.

Doewe Technologies is always committed to achieving innovative, unique, and reliable product solutions in the field of data acquisition. We deeply understand that these elements are the cornerstone for enterprises to establish themselves in market competition. For this reason, we derive innovative inspiration from customers' real application needs, rather than merely showcasing flashy product features. By continuously optimizing and enhancing data acquisition solutions, Doewe Technologies empowers partners to move towards an efficient and precise future. Welcome to choose Doewe Technologies (+86-10-64327909), and together open a new chapter in data acquisition.